# ZTE MW3736Hardware Design User Manual

**Version：V1.0**

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## Version update description

| Product version | Document version | Document No. | Document update descriptions |
|---|---|---|---|
| | V1.0 | | Released for the first time |
| | | | |
| | | | |

## Writer

| Document version | Date | Written by | Requested by | Approved by |
|---|---|---|---|---|
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# Preface

## Summary

This user manual mainly describes ZTE MW3736 module's product principle diagram, module's PINs, hardware interfaces and module structure. This manual is used to instruct the users on the module's hardware design, and on the basis of this module, quickly and conveniently design different kinds of wireless terminals.

## Target Readers

- System designing engineers
- Mechanical engineers
- Hardware engineers
- Software engineers
- Testing engineers

## Description of contents:

This manual contains 5 chapters. See the table below:

1. Module's General description. This chapter introduces MW3736 module's basic technical specification, relevant documents and abbreviations.

2. Module's External Interfaces. This chapter introduces MW3736 module's pin name and functions.

3. Module's Electrical Characteristics. This chapter describes MW3736 module's interface level, power consumption, reliability, etc.

4. Description of Hardware Interfaces. This chapter describes MW3736's hardware interfaces.

5. Mechanical Design. This chapter describes MW3736 module's appearance diagram, assembly diagram and PCB layout on the main board.


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# 1 Module's General Description

With 36-PIN stamp-hole interface, MW3736 module developed by ZTE Corporation is a kind of WCDMA/GSM industrial module, which can be built in the Set-Top-Box, vehicle-mounted terminals, and enable users to get access to the Internet wirelessly and send/receive Emails, browse the web pages, download at high speed and play online videos, etc.

It enables users to get access to the Internet any time in a place where WCDMA/GSM network is covered. It also features in SMS, voice call, etc. and provides highly free and convenient solutions for users in mobile data communication, and truly realizes the dream of mobile office.

MW3736 module is divided into two products with different frequency bands, respectively named as MW3736_V1A and MW3736_V1B. They can be recognized through the silkscreen printed at the bottom of it. MW3736_V1A corresponds to the frequency band WCDMA850/1900, GSM850/900/1800/1900; while MW3736_V1B corresponds to the frequency band WCDMA850/900/2100, GSM850/900/1800/1900.

This chapter mainly introduces the module's basic functions and logic block diagrams.

## 1.1 Introduction to Module's Functions

Table 1-1 Module's functions

| Parameters | MW3736 |
|---|---|
| Basic features | |
| Frequency band | WCDMA850/1900、GSM850/900/1800/1900(MW3736_V1A)<br>WCDMA850/900/2100、GSM850/900/1800/1900(MW3736_V1B) |
| Dimensions | 39.50mm×31.00mm×2.65mm |
| Weight | 10g |
| Work temperature | -25℃~+65℃ |
| Storage temperature | -30℃~+85℃ |
| Performance | |
| Work voltage | 3.3V~4.25V<br>Standard: 3.8V |
| Standard consumption | Sleep current (Min.): 1mA |
| | Idle current（Ave.）: 5mA@-75dBm |
| | Talk current: 230mA@-75dBm |
| | Maximum current (instantaneous value): 1800mA@-102dBm |
| Maximum output power | 22.5dBm ~ 30dBm@-102dBm |

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| Parameters | MW3736 |
|---|---|
| Rx. signal sensitivity | -108dBm |
| Interface | |
| Connection method | 36 Pin stamp-hole |
| Antenna | U.FL-R-SMT 50ohm antenna connector |
| Integrated full duplex port | AT command, data transmission |
| UIM card socket level | 1.8V /2.85V |
| Data service | |
| Mode | HSPA+/WCDMA/ GSM/EDGE |
| Max. downlink data rate | 14.4Mbps |
| Max. uplink data rate | 5.76Mbps |
| Protocol | Internal TCP/IP and UDP/IP protocol stack |
| | TCP server |
| | Embedded FTP |
| SMS | |
| | Support TEXT/PDU mode |
| | PTP MO/MT |
| | SMS Cell Broadcast |
| Audio (optional) | |
| | PCM audio |
| | Headset |
| | Audio encoder EVRC & 13K QCELP |
| | Volume control |
| | Support DTMF |
| AT command settings | |
| | Common AT commands |
| | ZTE exclusive AT commands |

## 1.2 Module's Principle Block Diagram

See MW3736's major logic functions in the following block diagram:


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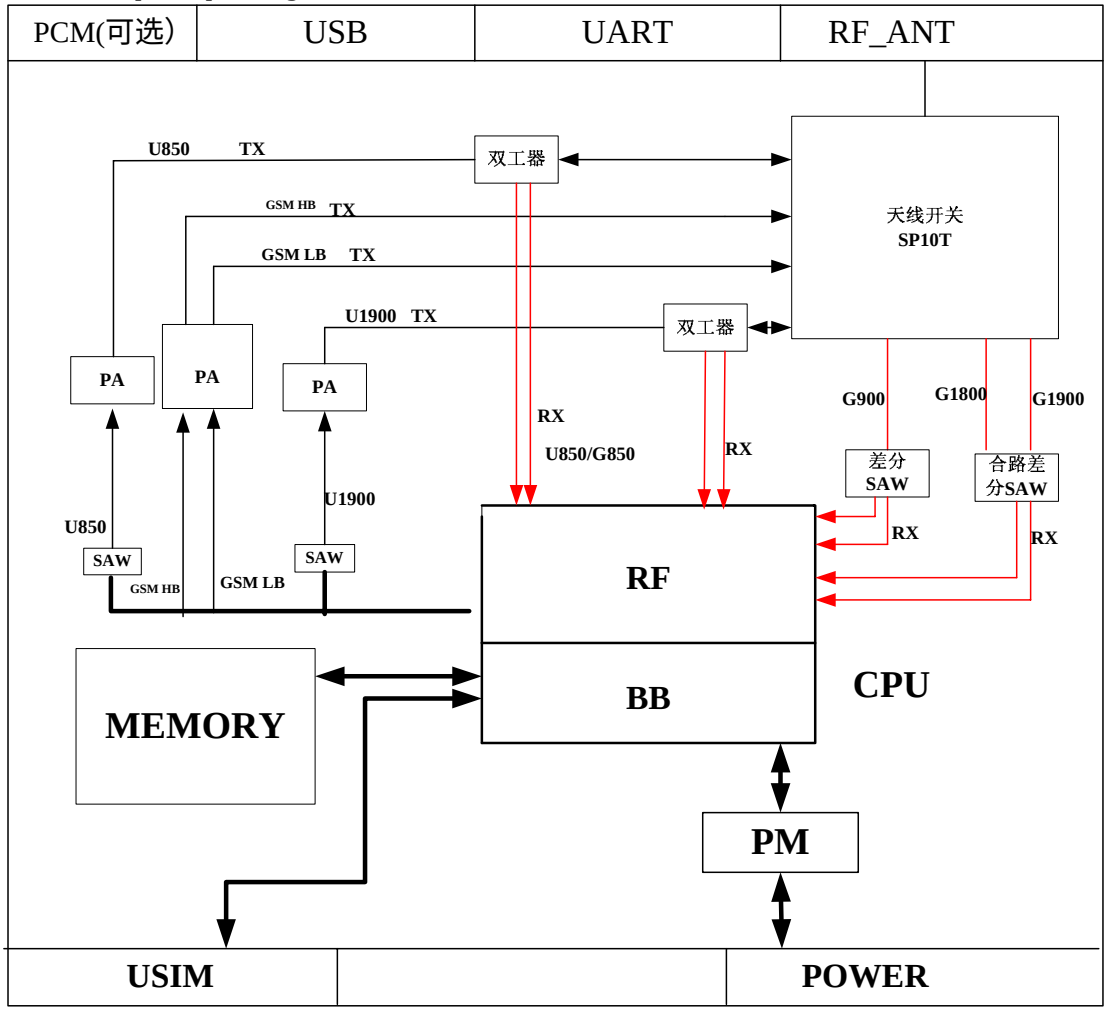
Figure 1-1 Module's principle diagram

MW3736_V1A principle diagram:

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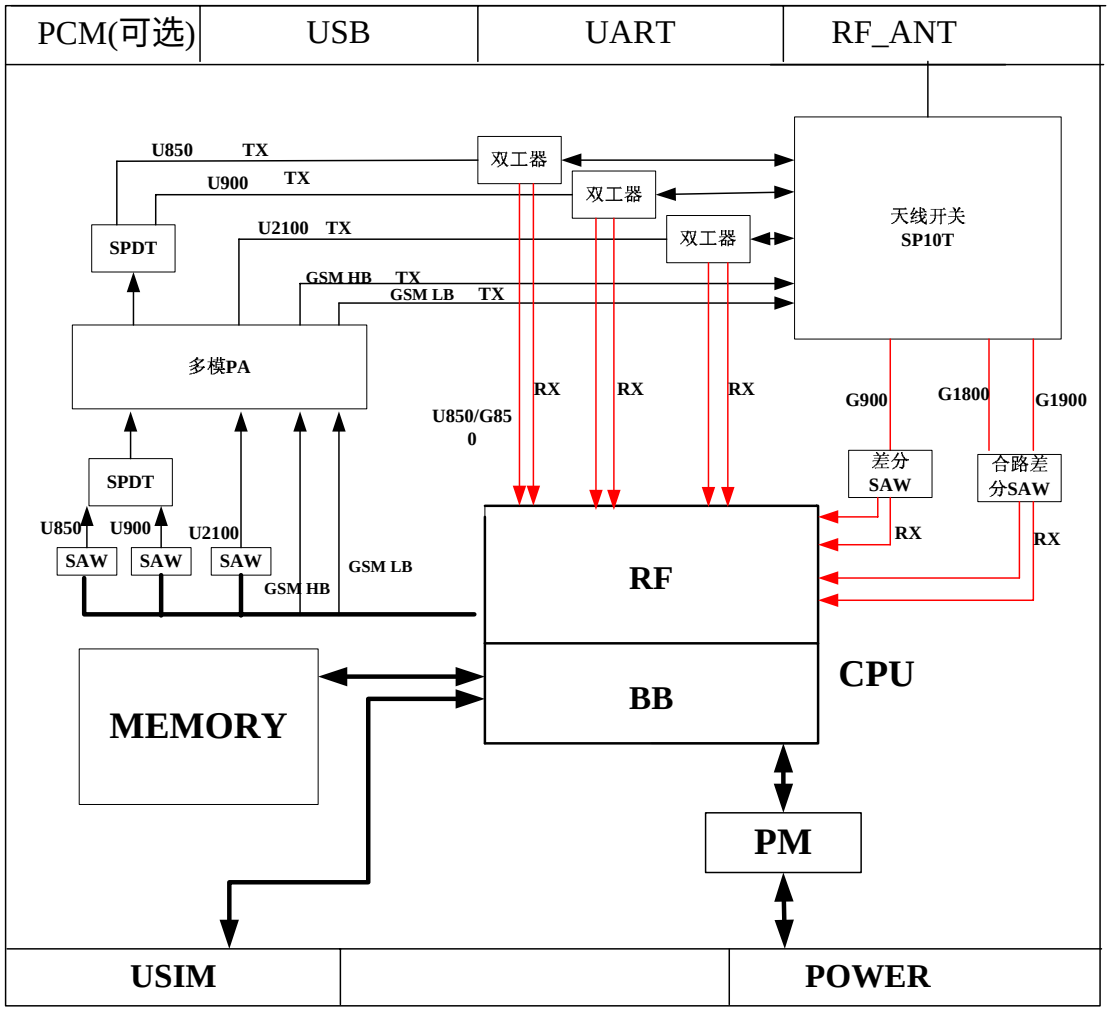
MW3736_V1B principle diagram:




## 1.3 Abbreviations

Table 1-2 Introduction to Abbreviations

| | | |
|---|---|---|
| A | | |
| ADC | Analog-Digital Converter | |
| AFC | Automatic Frequency Control | |
| AGC | Automatic Gain Control | |
| ARFCN | Absolute Radio Frequency Channel Number | |
| ARP | Antenna Reference Point | |
| ASIC | Application Specific Integrated Circuit | |
| B | | |
| BER | Bit Error Rate | |
| BTS | Base Transceiver Station | |
| C | | |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| | | |
|---|---|---|
| CDMA | Code Division Multiple Access | |
| CDG | CDMA Development Group | |
| CS | Coding Scheme | |
| CSD | Circuit Switched Data | |
| CPU | Central Processing Unit | |
| D | | |
| DAI | Digital Audio interface | |
| DAC | Digital-to-Analog Converter | |
| DCE | Data Communication Equipment | |
| DSP | Digital Signal Processor | |
| DTE | Data Terminal Equipment | |
| DTMF | Dual Tone Multi-Frequency | |
| DTR | Data Terminal Ready | |
| E | | |
| EFR | Enhanced Full Rate | |
| EGSM | Enhanced GSM | |
| EMC | Electromagnetic Compatibility | |
| EMI | Electro Magnetic Interference | |
| ESD | Electronic Static Discharge | |
| ETS | European Telecommunication Standard | |
| F | | |
| FDMA | Frequency Division Multiple Access | |
| FR | Full Rate | |
| G | | |
| GPRS | General Packet Radio Service | |
| GSM | Global Standard for Mobile Communications | |
| H | | |
| HR | Half Rate | |
| I | | |
| IC | Integrated Circuit | |
| IMEI | International Mobile Equipment Identity | |
| ISO | International Standards Organization | |
| ITU | International Telecommunications Union | |
| L | | |
| LCD | Liquid Crystal Display | |
| LED | Light Emitting Diode | |
| M | | |
| MCU | Machine Control Unit | |
| MMI | Man Machine Interface | |
| MS | Mobile Station | |
| P | | |
| PCB | Printed Circuit Board | |
| PCL | Power Control Level | |

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| | | |
|---|---|---|
| PCS | Personal Communication System | |
| PDU | Protocol Data Unit | |
| PLL | Phase Locked Loop | |
| PPP | Point-to-point protocol | |
| R | | |
| RAM | Random Access Memory | |
| RF | Radio Frequency | |
| ROM | Read-only Memory | |
| RMS | Root Mean Square | |
| RTC | Real Time Clock | |
| S | | |
| SIM | Subscriber Identification Module | |
| SMS | Short Message Service | |
| SRAM | Static Random Access Memory | |
| T | | |
| TA | Terminal adapter | |
| TDMA | Time Division Multiple Access | |
| TE | Terminal Equipment also referred it as DTE | |
| U | | |
| UART | Universal asynchronous receiver-transmitter | |
| UIM | User Identifier Management | |
| USB | Universal Serial Bus | |
| V | | |
| VSWR | Voltage Standing Wave Ratio | |
| Z | | |
| ZTE | ZTE Corporation | |


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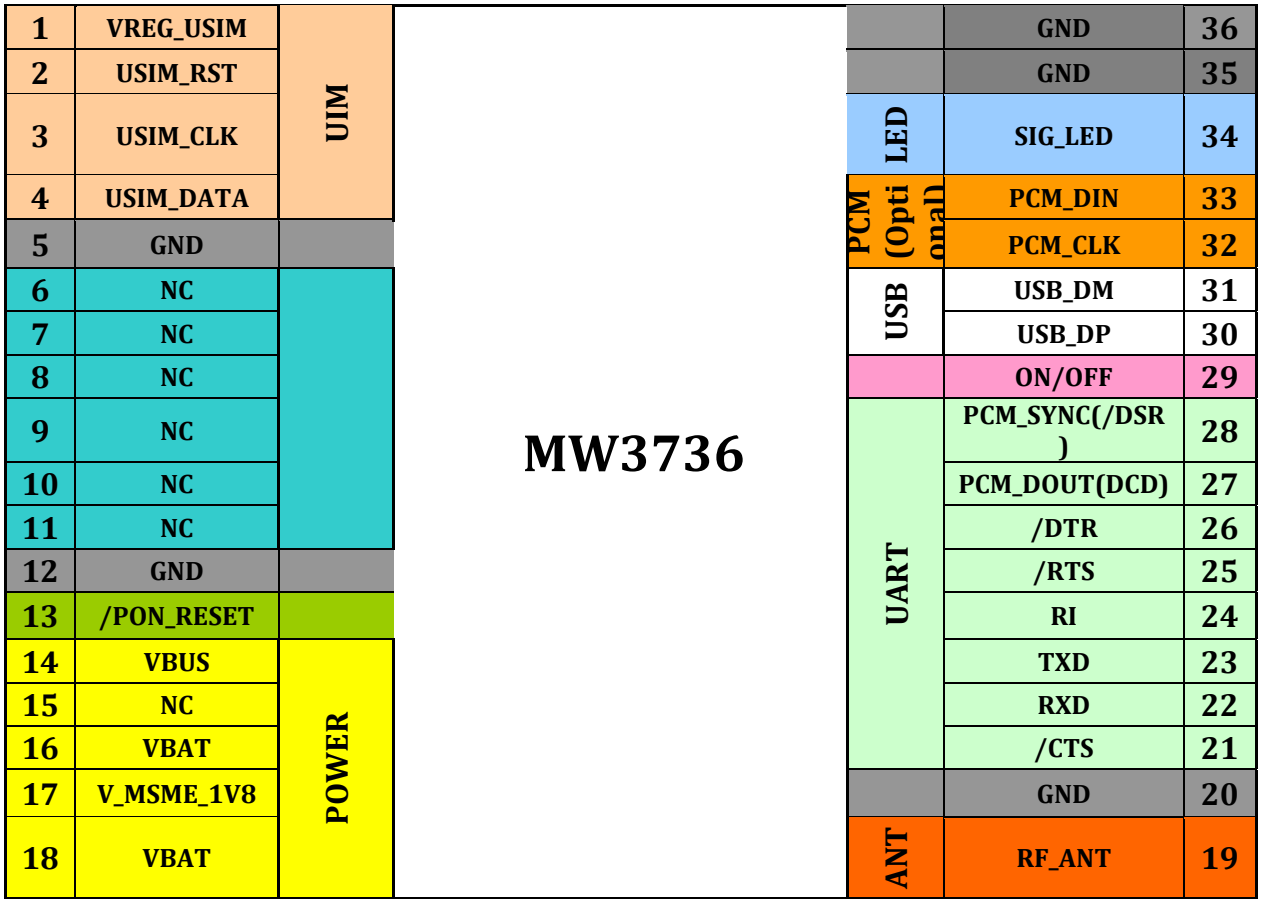
# 2 Description of Module's External Interfaces

MW3736 module adopts 36pin stamp-hole interface to connect externally.

## 2.1 Definitions of Module's Interfaces

Table 2-1 Definitions of module's interface




| Functions | Pin No. | Signal name | I/O | Basic functions | Remarks |
|---|---|---|---|---|---|
| SIM card interface | 1 | VREG_USIM | O | 2.85V/1.8V power supply | |
| | 2 | USIM_RST | O | USIM card reset signal | |
| | 3 | USIM_CLK | O | USIM card clock cable | |
| | 4 | USIM_DATA | I/O | USIM card data cable | |
| | 11 | MIC1_N | I | Differential audio input | |

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| | | | | | |
|---|---|---|---|---|---|
| | | | | channel1 - | |
| Reset | 13 | /PON_RESET | I | Reset signal | 1.8V, valid upon low level |
| Power | 14 | VBUS | I | USB power | +5V |
| | 16 | VBAT | I | Module's main power | 3.3V-4.2V |
| | 17 | V_MSME_1V8 | O | Digital power | Voltage output, 1.8V |
| | 18 | VBAT | I | Module's main power | 3.3V-4.2V |
| | 29 | ON/OFF | I | Power on/off control | 1.8V, valid upon low level |
| UART | 21 | /CTS | I | Clear to send | 1.8V, valid upon low level |
| | 22 | RXD | I | Receive data | 1.8V |
| | 23 | TXD | O | Transmit data | 1.8V |
| | 24 | RI | O | Ringtone | 1.8V |
| | 25 | RTS | O | Request to send | 1.8V, valid upon low level |
| | 26 | /DTR | I | Data terminal ready | 1.8V, valid upon low level |
| PCM **(optional)** | 27 | PCM_DOUT (DCD) | O | PCM data output | 1.8V，duplex with DCD |
| | 28 | PCM_SYNC (/DSR) | O | PCM frame SYNC clock | 1.8V，duplex with /DSR |
| | 32 | PCM_CLK (WAKEUP) | O | PCM data clock | 1.8V, duplexing pin. See Note (1) for detailed functions. |
| | 33 | PCM_DIN | I | PCM data input | 1.8V |
| USB interface | 30 | USB_DP | I/O | USB data+ | |
| | 31 | USB_DM | I/O | USB data- | |
| LED | 34 | SIG_LED | O | Module's working status indicator | |
| Antenna | 19 | RF_ANT | I/O | Antenna interface | |
| GND | 5<br>12<br>20 | GND | | | |


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| | | | | | |
|---|---|---|---|---|---|
| | 35<br>36 | | | | |

Note:

（1） The default function is WAKEUP, and generally it is at high level. After entering the USB sleep mode, the module needs to wake up the main controller (or PC) to trigger certain event (e.g., call or text message); in this case, it displays the level variation of “Low—High--Low”, and each state lasts for 1 second; after that, the PIN automatically becomes high level, and the main controller (or PC) needs to send USB wakeup command to awaken the module.

（2） As the PCM function is enabled, it’s used as the CLK pin of the PCM. As the module enters the sleep mode, there is high level at WAKEUP pin; when it needs to wake up the main controller (or PC) if there is an incoming call at this moment, it displays the level variation of “Low—High--Low”, and each state lasts for 1 second; subsequently it displays the waveform of the PCM CLK PIN. When it needs to wake up the main controller (or PC) if there is other event such as text message, it displays the level variation of “Low—High--Low”, and each state lasts for 1 second; subsequently the PIN automatically becomes high level

## 2.2 Antenna Interface

Proper measures should be taken to reduce the access loss of effective bands, and good shielding should be established between external antenna and RF connector. Besides, external RF cables should be kept far away from all interference sources such as high-speed digital signal or switch power supply.

According to mobile station standard, stationary wave ratio of antenna should be between 1.1 and 1.5, and input impedance is 50 ohm. Different environments may have different requirements on the antenna’s gain. Generally, the larger gain in the band and smaller outside the band, the better performance the antenna has. Isolation degree among ports must more than 30dB when multi-ports antenna is used. For example, between two different polarized ports on dual-polarized antenna, two different frequency ports on dual-frequency antenna, or among four ports on dual-polarized dual-frequency antenna, isolation degree should be more than 30dB.

Precautions of using PIN2 and RF connector:

Compatible design has been used on MW3736 RF external interface, therefore customers can select reasonably according to the product form during the second-time development of the module to optimize the cost of BOM.

Program 1：

PIN2 is used as the antenna PIN. Pay attention to the following when using it as the antenna’s feed PIN:

（1）The feed connected to PIN2 is 50ohm micro-strip or strip line. To approach the module, put π shape or F shape matching network for later tuning.

（2）The RF wires must be kept away from the GND, and generally the distance should be 3 times of the width of RF wires.

（3）It’s forbidden to put some interference sources such as DCDC, WIFI module around RF wires

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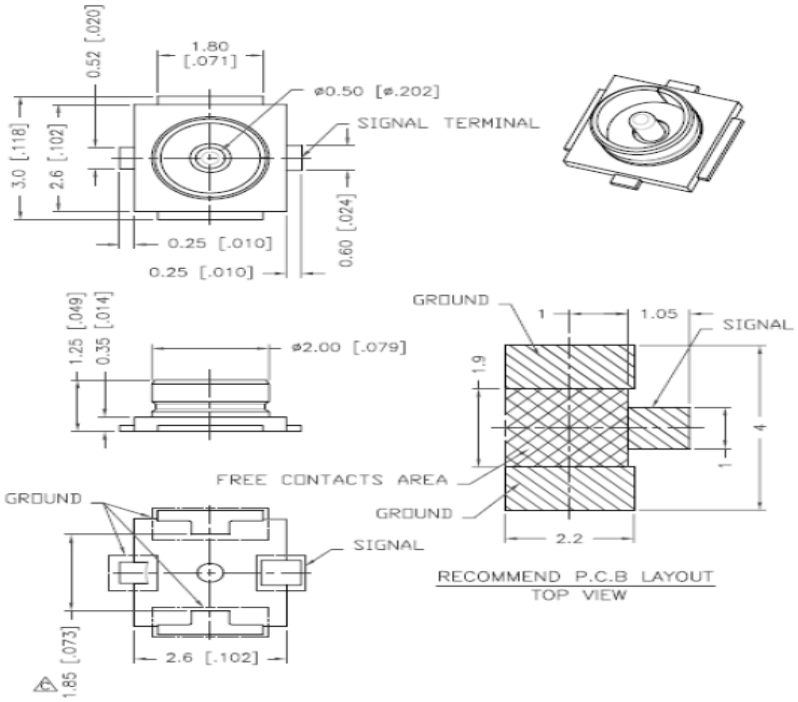
or RF port

Program 2:

When using RF plug as the antenna feed, disconnect PIN2 from the main board and make sure there are some clean areas below or around PIN2. Keep 2mm distance between the surface of PIN2 and GND, and drill holes below PIN2. It's not suggested to use the compatible design of PIN2 at the same time when using the RF connector.

Figure 2-1 Antenna interface diagram




## 2.3 Antenna Interface's RF Performance

See the antenna interface's RF performance in table 2-2:

Table 2-2 Antenna Interface's RF Performance

MW3736_V1A:

| Antenna Interface's RF Performance | Module's uplink (MS->BTS) | Module's downlink (BTS->MS) | Power (dBm) | Antenna interface Rx. sensitivity |
|---|---|---|---|---|
| WCDMA850 | 824MHz-849MHz | 869MHz-894MHz | 23±2 | < -110dBm |
| WCDMA1900 | 1850MHz-1910MHz | 1930MHz-1990MHz | 23±2 | < -110dBm |
| GSM850 | 824MHz-849MHz | 869MHz-894MHz | 33±2 | < -108dBm |
| GSM900 | 880MHz-915MHz | 925MHz-960MHz | 33±2 | < -108dBm |
| GSM1800 | 1710MHz-1785MHz | 1805MHz-1880MHz | 30±2 | < -108dBm |
| GSM1900 | 1850MHz-1910MHz | 1930MHz-1990MHz | 30±2 | < -108dBm |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MW3736_V1B:

| Antenna Interface's RF Performance | Module's uplink (MS->BTS) | Module's downlink (BTS->MS) | Power (dBm) | Antenna interface Rx. sensitivity |
|---|---|---|---|---|
| WCDMA850 | 824MHz-849MHz | 869MHz-894MHz | 23±2 | < -110dBm |
| WCDMA900 | 880MHz-915MHz | 925MHz-960MHz | 23±2 | < -110dBm |
| WCDMA2100 | 1920MHz-1980MHz | 2110MHz-2170MHz | 23±2 | < -110dBm |
| GSM850 | 824MHz-849MHz | 869MHz-894MHz | 33±2 | < -108dBm |
| GSM900 | 880MHz-915MHz | 925MHz-960MHz | 33±2 | < -108dBm |
| GSM1800 | 1710MHz-1785MHz | 1805MHz-1880MHz | 30±2 | < -108dBm |
| GSM1900 | 1850MHz-1910MHz | 1930MHz-1990MHz | 30±2 | < -108dBm |

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# 3 Module's Electrical Characteristics

This chapter mainly introduces the module's electrical characteristics, including module's interface level, power consumption, reliability, etc.

## 3.1 Descriptions of interface level

Table 3-1 Description of level of module's main external interfaces

| External interfaces | High/low level | Min. | Typical | Max. | Remarks |
|---|---|---|---|---|---|
| UART | 0 | | 0 | 0.3*V_UART | |
| | 1 | 0.7*V_UART | V_UART | | Internal voltage conversion |
| UIM | 0 | | 0 | 0.3*VREG_RUIM | |
| | 1 | 0.7*VREG_RUIM | VREG_RUIM | | |

Among them, V_UART is 1.8V, and VREG_RUIM is 1.8V/2.85V.

## 3.2 Power on/off Time Sequence

The time sequence diagram indicates the whole power on/off process.


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Figure 3-1 Power on/off time sequence diagram

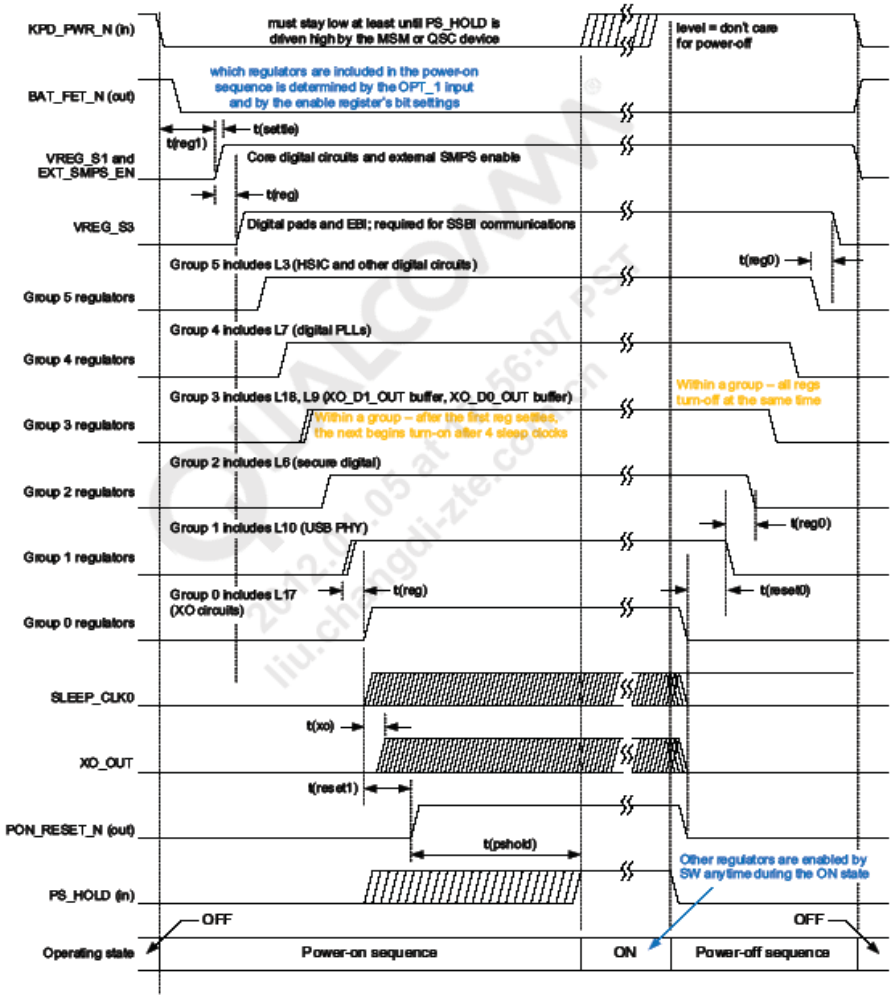
KPD_PWR_N (in)
must stay low at least until PS_HOLD is driven high by the MSM or QSC device
level = don't care for power-off
BAT_FET_N (out)
which regulators are included in the power-on sequence is determined by the OPT_1 input and by the enable register's bit settings
t(reg1)
t(settle)
VREG_S1 and EXT_SMPS_EN
Core digital circuits and external SMPS enable
t(reg)
VREG_S3
Digital pads and EBI; required for SSBI communications
Group 5 includes L3 (HSIC and other digital circuits)
t(reg0)
Group 5 regulators
Group 4 includes L7 (digital PLLs)
Group 4 regulators
Group 3 includes L18, L9 (XO_D1_OUT buffer, XO_D0_OUT buffer)
Within a group – all regs turn-off at the same time
Group 3 regulators
Within a group – after the first reg settles, the next begins turn-on after 4 sleep clocks
Group 2 includes L6 (secure digital)
Group 2 regulators
Group 1 includes L10 (USB PHY)
t(reg0)
Group 1 regulators
Group 0 includes L17 (XO circuits)
t(reg)
t(reset0)
Group 0 regulators
SLEEP_CLK0
t(xo)
XO_OUT
t(reset1)
PON_RESET_N (out)
t(pshold)
Other regulators are enabled by SW anytime during the ON state
PS_HOLD (in)
OFF
OFF
Operating state
Power-on sequence
ON
Power-off sequence

Table 3-2 Power on/off circuit time characteristics

| Parameter | Comments | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| Internal pull-up resistor [1] | At KPD_PWR_N | – | 200 | – | kΩ |
| Sequence time intervals [2] | | | | | |
| t(reg1) | Poweron event to first regulator on [3] | 26 | 33 | 40 | ms |
| t(reg) | Time for regulator to settle before next enable | 100 | 128 | 500 | µs |
| t(settle) | Regulator settling time [4] | 20 | – | 500 | µs |
| t(xo) | XO regulator enable to valid XO pulses | – | – | 6 | ms |
| t(reset1) | Last regulator on to PON_RESET_N = H | 10 | 20 | 30 | ms |
| t(pshold) | PS_HOLD timeout | 133 | 200 | 300 | ms |
| t(reset0) | PON_RESET_N = L to first regulator in group 1 off | 6.7 | 10.0 | 15 | ms |
| t(reg0) | Time allowed for discharge | – | – | 2 | ms |
| Regulator accuracy | To continue poweron sequence | 4 | 7 | 9 | % |
| Debounce timer [5] | | 15.625 | – | 2000 | ms |
| Power supply current | | | | | |
| Normal operation | | – | 10 | 12 | µA |
| Off | | – | 2 | 5 | µA |

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## 3.3 Reliability

Before leaving the factory, the module has gone through a series of reliability tests, such as: high/low temperature operation, high/low temperature storage, thermal shock, alternating temperature humidity, etc. The test results conform to the requirements in the industry. List the module's work temperature in the table below:

Table 3-3 Module's temperature characteristics

| Parameters | Descriptions | Min. | Max. | Remarks |
|---|---|---|---|---|
| To | Normal work temperature | -25℃ | +65℃ | |
| Ta | Limited work temperature | -30℃ | +75℃ | Basic functions are normal, but the RF performance slightly drops. |
| Ts | Module's storage temperature | -40℃ | +85℃ | |

## 3.4 ESD

The module's interface, antenna interface and UIM card interface all pass the standard ESD performance testing.

Table 3-4 Module's ESD characteristics

| Interface | Test items | Test requirements | Performance |
|---|---|---|---|
| Antenna interface | Air discharging | ±8 kV | Nothing wrong |
| | Contact discharging | ± 6 kV | Nothing wrong |
| UIM card interface | Air discharging | ±8 kV | Nothing wrong |
| | Contact discharging | ± 6 kV | Nothing wrong |


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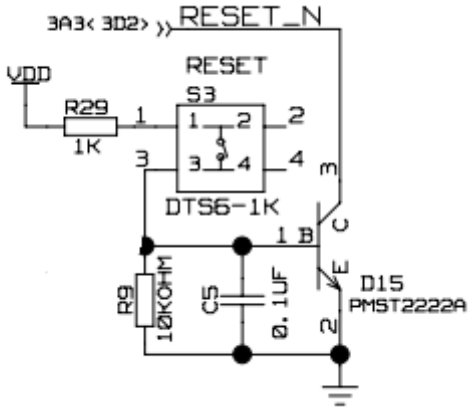
# 4 Reference Design of Interface Circuits

This chapter describes the reference design of interface circuits and precautions according to the module's functions.

## 4.1 Power and Reset

See the reference design of power circuit in figure 4-1.

Figure 4-1 Power and reset circuit reference design diagram




- Power design

The module is powered by VBAT. See the voltage characteristics in table 4-1.

Table 4-1 Voltage characteristics

| Classification | MIN | TYPICAL | MAX（instantaneous） |
|---|---|---|---|
| Input voltage | 3.3 V | 3.8 V | 4.2 V |
| Input current | < 3mA (average) | -- | 530mA（WCDMA）<br>1800mA（GSM） |

- Power on

The module will be normally powered off after connected to the power normally.

Provide one 4S ~ 6S low pulse to the module's ON/OFF pin to turn on the module.

The time required to power on at each time depends on the module's status. Usually, the low level must last for at least 4 seconds.

- Power off

Provide one 4S ~ 6S low pulse to the module's ON/OFF pin to turn off the module.

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- Reset

Provide one 3S low pulse to the module's /RESET pin to reset the module.

After reset, the module will enter the power-off status. Provide one at least 4S low pulse to the module's ON/OFF pin to turn on the module again.

V_MSME_1V8

There is a voltage output pin with current adjuster on MW3736 module, which can be used to supply external power to the board. The voltage of this pin and the voltage of baseband processor/memory come from the same voltage adjuster. The voltage output is available only when the module is on. The normal output voltage is 1.8V, and the user should absorb the current from this pin as little as possible (less than 10mA). Generally, it is recommended to use this pin for pull-up when matching the level.

Other Advice

In order to make sure the data is saved safely, please don't cut off the power when the module is on. It's strongly recommended to use the soft switch to turn off the mobile phone. If the interval between the cut-off and power-on is less than 2 seconds, it would cause the module to automatically power on.

## 4.2 COM Port

The module provides a full duplex UART interface, whose maximal data rate is 230.4kbps and typical data rate is 115.2kbps. The external I/O level is 1.8V CMOS signal.

Precautions：

1）The module's I/O level is 1.8V CMOS, and the level conversion is required when connected with standard 3.3V logic circuit.(e.g., MCU or RS232 driver chip MAX3238). Otherwise, it might cause unstable com ports because the level is not matched or cause damage to the module because it is at high level for a long time.

For non 1.8V external UART, it needs to convert the level. Normally a dynatron is used to realize the level conversion. As shown in figure 4-2, the resistance is just for your information, please calculate again during the design. The diode in the figure is Schottky diode (forward voltage drop: 0.3V). If you select other diode, please select one with smaller forward voltage drop to guarantee that RXD_1V8's level is below the threshold when inputting low level.

2）Port baud rate 115200 (by default), can be used for AT commands and MODEM. The hard flow control is OFF by default.


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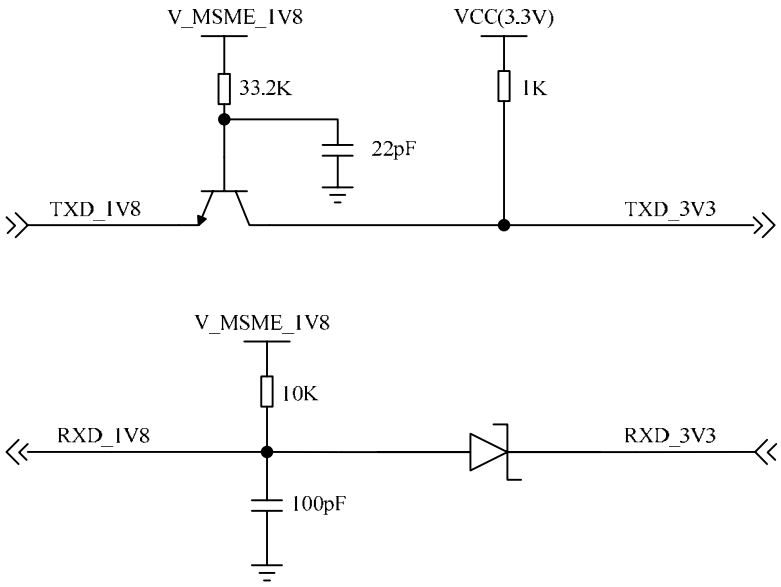
Figure 4-2 UART interface level conversion




4) Connect to RXD and TXD only when there is no flow control in use;

When using hardware flow control to connect other processors, use RXD, TXD, /CTS and /RTS; when used as Modem to connect to the PC, connect all IO signal cables (8 wires). Besides, the ringtone signal will produce low level interruption upon an incoming call or text message. Select the port IO signals for level conversion according to the specific conditions.

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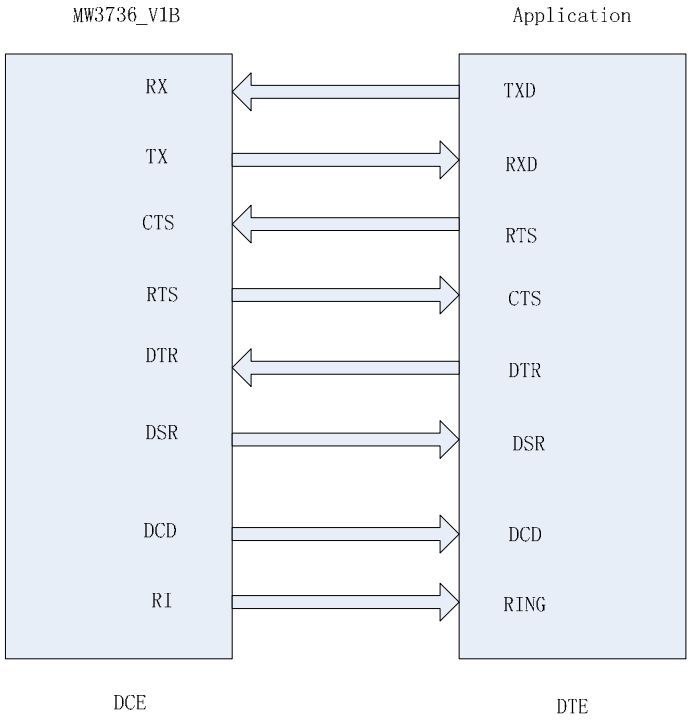
Descriptions of UART interface:

Figure 4-3 UART DCE－DTE connection relationship diagram




See the definitions of UART1 interface in table 4-2.

Table 4-2 Definitions of UART1 interface

| Classification | No. | Definitions | I/O | Descriptions | Remarks |
|---|---|---|---|---|---|
| UART (1.8V) | 22 | UART_RX | I | Receive data | DTE transmits serial data |
| | 25 | UART_RTS | O | Ready to send | DTE informs DCE to send |
| | 23 | UART_TX | O | Transmit data | DTE receives serial data |
| | 26 | UART_DTR | I | Data terminal ready | DTE is ready |
| | 21 | UART_CTS | I | Clear to send | DCE has switched to Rx. mode |
| | 24 | UART_RI | O | Ringtone indication | Inform DTE upon a remote call |
| | 28 | UART_DSR | O | Data set ready | DCE is ready |
| | 27 | UART_DCD | O | Carrier wave detection | Data link connected |
| | | GND | | GND | |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## 4.3 UIM card Interface

The module supports 1.8V/2.85V UIM card. See the design in figure 4-3. It's recommended to add ESD to protect the UIM card.

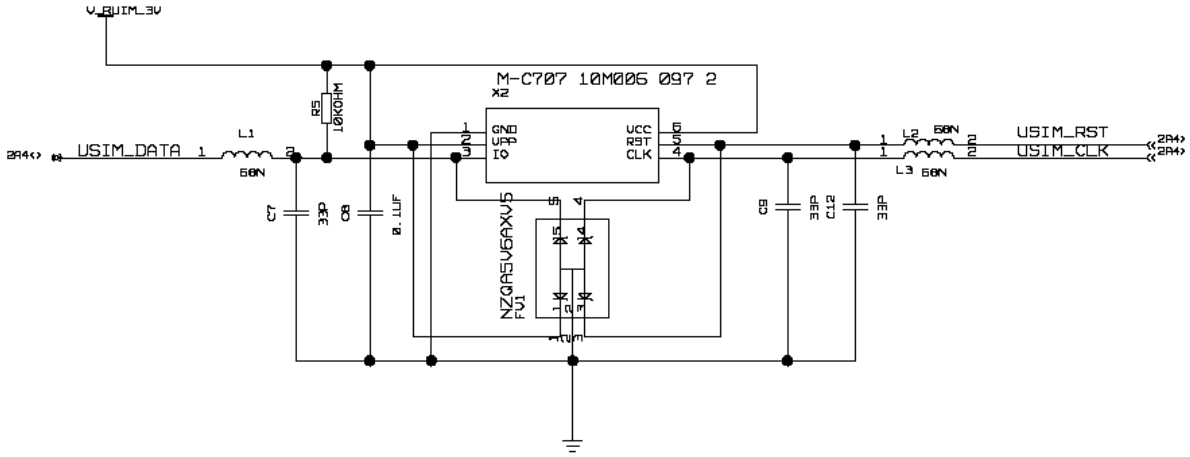
Table 4-3 UIM card interface definitions

| Classification | No. | Definitions | I/O | Descriptions | Remarks |
|---|---|---|---|---|---|
| UIM | 1 | V_RUIM | O | RUIM card voltage | |
| | 2 | UIM_RST | O | RUIM card rest | |
| | 3 | UIM_CLK | O | RUIM card clock | |
| | 4 | UIM_DATA | I/O | RUIM card data | |

The typical rate value of UIM card interface is about 3.25MHz, therefore the UIM card socket should be put near the module's interface to avoid serious waveform deformation caused by overlong wiring (it's advised that the wiring should not exceed 100mm), otherwise, it will affect the signal communication.

The wiring of UIM_CLK and USIM_DATA should be enveloped by the ground wires. Add one 0.1uF or 0.22uF capacitance to V_RUIM, and add 33pF capacitance to UIM_CLK, UIM_DATA & UIM_RST to filter the interference of antenna signals. Besides, the anti-static performance of these four signals can be realized through the TVS tube or ESD component. See the figure below for the reference design.

Figure 4-4 UIM card circuit reference design




Note:

The PCB wiring of UIM card should be laid closely around the module as possible as you can, and the ESD component should be put near the UIM card socket.

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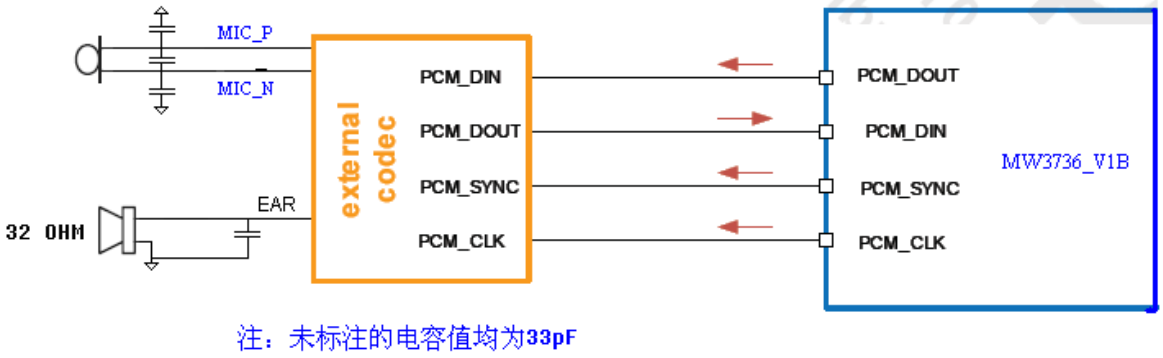
## 4.4 Audio Interface (optional)

The module provides one PCM interface, which must connect one CODEC externally to input and output audios. The module's PCM interface provides PCM_CLK, PCM_SYNC, PCM_DIN, PCM_DOUT，and it supports 2.048MHz PCM clock data rate and 8K frame data rate. PCM clock will stop the output when it enters the dormant mode.

The module's PCM interface must work under Master mode, and the clock and SYNC signal must be sent by the module. The device connected with the interface can work under Slave mode only.

See the audio interface circuit in figure 4-4.

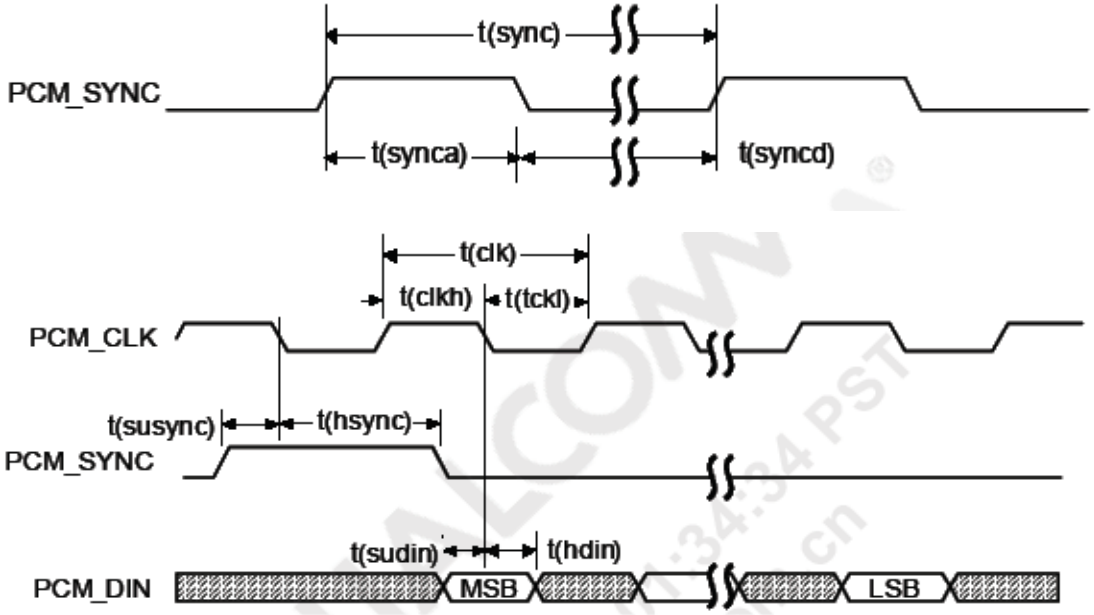
Figure 4-5 Audio interface circuit reference design principle diagram




- Codec audio interface design on the headset

The two microphone interfaces MIC_N and MIC_P are both differential interfaces, which could also be used for single-end input. It's recommended to use differential mode to reduce the noises. Refer to the connection of EAR left/right channel in the figure.

See the time sequence of PCM interface in figure 4-5.





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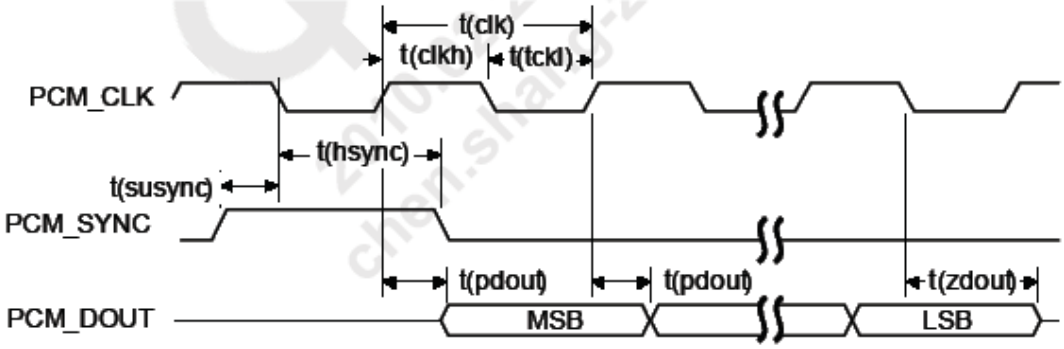



| Parameter | | Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| t(sync) | PCM_SYNC cycle time | | – | 125 | – | µs |
| t(synca) | PCM_SYNC asserted time | | – | 488 | – | ns |
| t(syncd) | PCM_SYNC de-asserted time | | – | 124.5 | – | µs |
| t(clk) | PCM_CLK cycle time | | – | 488 | – | ns |
| t(clkh) | PCM_CLK high time | | – | 244 | – | ns |
| t(clkl) | PCM_CLK low time | | – | 244 | – | ns |
| t(sync_offset) | PCM_SYNC offset time to PCM_CLK falling | | – | 122 | – | ns |

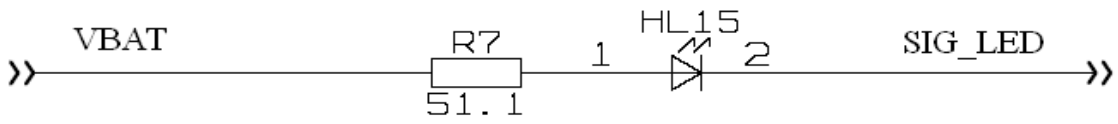
## 4.5 Work Status Indicators

The SIG_LED PIN output status is defined by the software. The SIG_LED PIN is MPP port, which can drive 20mA current. See the reference design of indicators in figure 4-5.

Table 4-4 Description of work status indicators

| Module status | Indicator status | Frequency |
|---|---|---|
| Power-on status | Slow flash | 1Hz |
| Network searching status | Standard flash | 3Hz |
| IDLE status | Slow flash | 1Hz |
| Traffic status | Fast flash | 5Hz |

Figure 4-5 Indicator reference design principle diagram

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# 5 Mechanical Design

## 5.1 Appearance Diagram

See MW3736 module's appearance in figure 5-1.

Figure 5-1 MW3736 module's appearance diagram

- Dimensions: 39.50mm×31.00mm×2.65mm
- Weight: 10g


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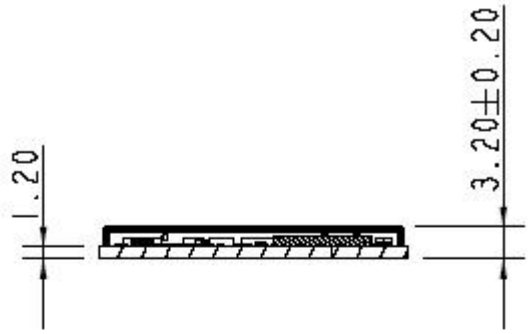
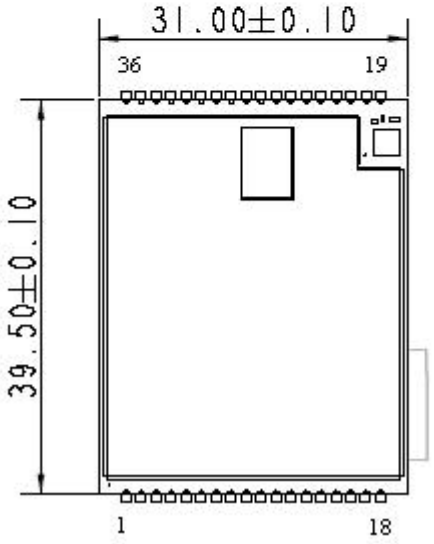
## 5.2 Module's Assembly Diagram

See the assembly diagram of the module in figure 5-2.

Figure 5-1 Module's assembly diagram

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## 5.3 Module's PCB Encapsulation Dimensions

See the module's PCB encapsulation dimensions in figure 5-3.

Figure 5-2 PCB encapsulation diagram of relevant female socket (top view)

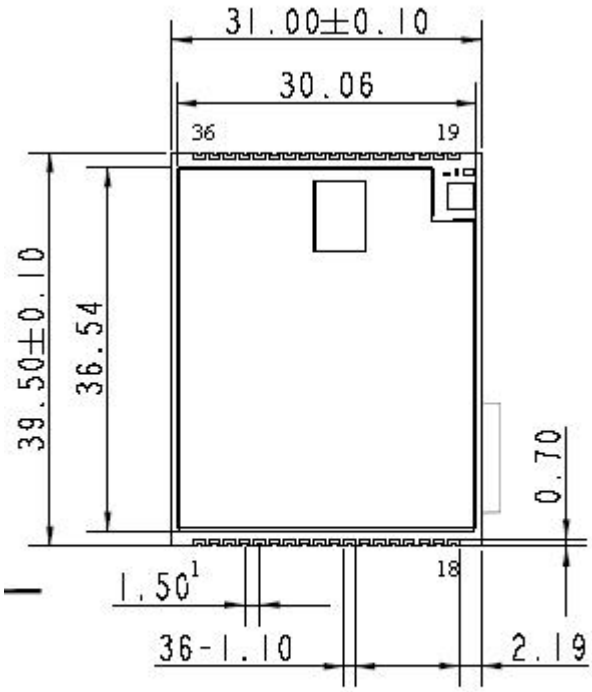



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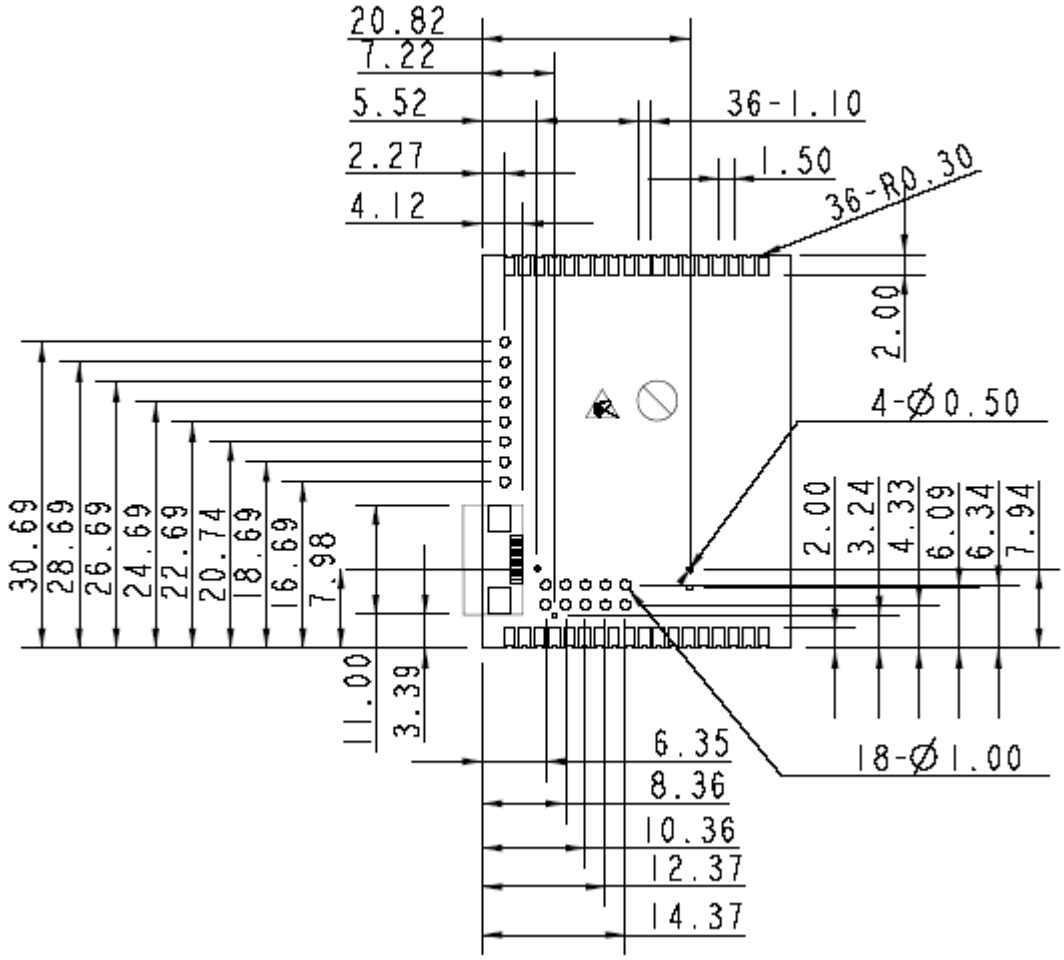
Figure 5-4 PCB encapsulation diagram of relevant female socket (bottom view)




Precautions while designing PCB:

1） Copper-clad and wiring are forbidden on each layer of the PCB at the area below the RF test points.

2） For the convenience of testing and maintenance, it might be necessary to drill holes on the PCB to expose J-TAG test points.

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